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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SON HO, KEVIN H. TONTHAT,
HAI-HOA VAN, and JOSEPH SHEREDY

Appeal 2009-005096
Application 10/646,289¹
Technology Center 2100

Decided: May 13, 2010

Before JOHN A. JEFFERY, JAY P. LUCAS, and THU A. DANG,
Administrative Patent Judges.

Opinion for the Board filed by JEFFERY, *Administrative Patent Judge.*

Opinion Dissenting filed by DANG, *Administrative Patent Judge.*

¹ We note that an appeal of related U.S. Patent Application No. 10/626,507 (App. Br. 3) has been decided by a different panel. *See Ex parte Ho*, No. 2009-005314 (BPAI Feb. 23, 2010) (non-precedential). The issues in that appeal, however, are different than those before us in this appeal.

DECISION ON APPEAL

Appellants appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1, 2, 4-7, 9, 10, 12-15, and 17-33. Claims 3, 8, 11, and 16 have been canceled. *See* App. Br. 20, 21, 23, and 24. We have jurisdiction under 35 U.S.C. § 6(b). We reverse.

STATEMENT OF THE CASE

Appellants invented a memory storage system that includes a memory device for storing data in a line cache when a miss occurs and improves the performance of the line cache under certain conditions. *See generally* Spec. 2 and 25; Fig. 24. We reproduce claim 1 below with the key disputed limitations emphasized:

1. A memory storage system that is accessed by a first central processing unit (CPU), comprising:

a line cache including a plurality of pages that are accessed by the first CPU;

a first memory device that stores data that is loaded into said line cache *when a miss occurs*,

wherein when said miss occurs and before a second miss occurs, n pages of said line cache are loaded with data from sequential locations in said first memory device, wherein n is greater than one;

a second memory device; and

a line cache control system that controls data flow between said line cache, the first CPU, said first memory device and said second memory device, and that includes:

a first line cache interface that is associated with the first CPU, that receives a first program read request from the first CPU and that generates a first address from said first program read request;

a first memory interface that communicates with said first memory device;

a second memory interface that communicates with said second memory device; and

a switch that selectively connects said line cache to one of said first and second memory interfaces, wherein when said line cache receives said first address, said line cache control system compares said first address to stored addresses in said line cache, returns data associated with said first address if a match occurs, and loads said n pages of said line cache when said miss occurs.

The Examiner relies on the following as evidence of unpatentability:

Alexander ²	US 6,131,155	Oct. 10, 2000
Zaidi	US 6,601,126 B1	July 29, 2003 (filed May 2, 2000)
Barroso	US 6,725,334 B2	April 20, 2004 (filed June 8, 2001)
Loafman	US 2005/0021916 A1	Jan. 27, 2005 (filed July 24, 2003)
Jeddeloh	US 7,133,972 B2	Nov. 7, 2006 (filed June 7, 2002)

² Alexander has not been listed by the Examiner in the Evidence Relied Upon section (Ans. 3) but has been discussed within the rejection. *See* Ans. 11-13.

THE REJECTIONS

1. The Examiner rejected claims 1, 2, 5-7, 10, 13-15, 18, 19, and 25 under 35 U.S.C. § 103(a) as unpatentable over Zaidi, Jeddelloh, and Loafman. Ans. 3-9.³

2. The Examiner rejected claims 4, 9, 12, 17, 26, 27,⁴ and 33 under 35 U.S.C. § 103(a) as unpatentable over Zaidi, Jeddelloh, Loafman, and Barroso. Ans. 9-11.

3. The Examiner rejected claims 20-24 under 35 U.S.C. § 103(a) as unpatentable over Zaidi, Jeddelloh, Loafman, and Alexander. Ans. 11-12.

4. The Examiner rejected claims 28-32 under 35 U.S.C. § 103(a) as unpatentable over Zaidi, Jeddelloh, Loafman, Barroso, and Alexander. Ans. 12-13.

THE CONTENTIONS

The Examiner finds that Zaidi and Jeddelloh collectively teach all the limitations of independent claim 1, except loading “n” pages of cache line with the miss and before a second miss occurs. Ans. 4-6. Loafman has been cited to teach this missing limitation. Ans. 6-7. While acknowledging that Loafman does not explicitly teach loading pages before a second miss occurs, the Examiner concludes Loafman suggests loading pages when a first miss occurs to reduce the number of page faults and latency. *Id.*

³ Throughout this opinion, we refer to (1) the Appeal Brief filed March 6, 2008; (2) the Examiner’s Answer mailed April 29, 2008; and (3) the Reply Brief filed June 30, 2008.

⁴ Claim 27 does not appear in the rejection’s heading (Ans. 9) but is discussed in the body of the rejection (Ans. 10-11). We therefore deem this error harmless.

Appellants argue that Loafman teaches prefetching or loading data after two misses occur, and not before a second miss occurs. App. Br. 9-12.

The issue before us, then, is as follows:

ISSUE

Under § 103, has the Examiner erred in rejecting independent claim 1 by finding that Zaidi, Jeddeloh, and Loafman collectively would have taught or suggested a memory storage system in which pages of line cache are loaded in a first memory device with data from sequential locations “when said miss occurs and before a second miss occurs”?

FINDINGS OF FACT (FF)

1. The Specification does not define “a miss” or “a second miss.”
See generally Specification.
2. The Specification discusses a look ahead method 500 that loads *n* pages of the line cache with the data located in sequential memory locations when a miss occurs. The Specification explains the look ahead method 500 ensures “there will never be a miss after the initial miss” as long as the central processing unit (CPU) continues to access sequential memory locations. Spec. ¶¶ 0090, 0093; Fig. 24.
3. Loafman discloses in the Background of the Invention section a read-ahead or data pre-fetching technique that is said to work “splendidly” for reading data sequentially. Loafman explains that pre-fetching involves obtaining data before needed, and reduces the number of page faults that may occur during a program’s execution. Loafman, ¶¶ 0010-12.

4. Loafman discusses pre-fetching a block of sequentially-read pages after two consecutive page faults. Loafman's virtual memory manager (VMM) 112 pre-fetches the next two successive pages (i.e., pages 206 and 208 of block pages 210) when the program accesses two successive pages of data (i.e., pages 202 and 204) each using a page fault. Loafman, ¶¶ 0008, 0012, and 0026; Fig. 2.

5. Loafman's VMM 112 loads data into memory after one page fault when randomly reading data. Loafman explains that this process continues as customary if the file is read sequentially. Loafman, ¶¶ 0027-32 and 0037-38; Fig. 3.

PRINCIPLES OF LAW

“[W]ith original examination, the PTO must give claims their broadest reasonable construction consistent with the specification.” *In re Suitco*, No. 2009-1418, 2010 WL 1462294, at *3 (Fed. Cir. Apr. 14, 2010) (internal quotations and citation omitted). When a claim uses the open-ended term, “comprising,” “this court has instructed that any such construction be consistent with the specification . . . and that the claim language should be read in light of the specification as it would be interpreted by one of ordinary skill in the art.” *Id.* at *4 (citations, internal quotation marks, and emphasis omitted).

ANALYSIS

We begin by construing the key disputed limitation of claim 1 which calls for, in pertinent part, “when a miss occurs, wherein when said miss occurs and before a second miss occurs, n pages of said line cache are

loaded with data from sequential locations in said first memory device” The Specification does not define “a miss” or “a second miss.” FF 1. Nonetheless, the Specification discusses a look-ahead method that loads the line cache’s pages with data from sequential memory locations or sequentially when a miss occurs. FF 2. In this context, the Specification further explains this method ensures “there will never be a miss after the initial miss.” *Id.* Thus, giving the phrase, “when said miss occurs and before a second miss occurs” its broadest reasonable construction in light of the Specification, we find “a miss” means a first or initial miss since another or second miss never occurs. *See Suitco*, 2010 WL 1462294, at *3. Also, consistent with the Specification, the broadest but reasonable construction of “a second miss” would be the next possible miss because, as the Specification explains (FF 2), there are no other misses. *See id.*

Although claim 1 uses the open-ended term “comprising,” construing these “misses” in any other sequence (e.g., construing (1) “a miss” as a second or subsequent miss, and (2) “a second miss” as a third or subsequent miss) would be inconsistent with the Specification and therefore unreasonable. *See Suitco*, 2010 WL 1462294, at *4. Although the Dissent proposes a different—and indeed interesting—construction of the recited “miss” limitations, *see op.* at 12-14, we nonetheless find our construction to be the broadest reasonable construction when interpreting these limitations in light of the Specification.

That said, we recognize that we should not import limitations from the Specification into the claims in arriving at our construction. *See Phillips v. AWH Corp.*, 415 F.3d 1303, 1323 (Fed. Cir. 2005) (en banc). But ultimately, it is the construction that stays true to the claim language and

most naturally aligns with the Specification's description of the invention that will be, in the end, the correct construction. *Id.* at 1316. And in the end, our construction of the "miss" limitations in claim 1 more reasonably comports with that mandate.

With this construction in mind, we turn to Loafman. Loafman discusses a pre-fetching or loading process that obtains data before necessary. FF 3. Specifically, Loafman provides an example of loading data sequentially or from sequential locations after two consecutive page faults or two misses. FF 4. As the Examiner admits (Ans. 6), however, Loafman does not explicitly teach loading pages in the first memory device from sequential locations after *only one miss* occurs.

Nonetheless, the Examiner contends that Loafman suggests loading pages when one miss occurs and before a second miss occurs. *See* Ans. 6-8 and 14-17. The Examiner's position is not completely without basis. That is, Loafman discusses loading the entire range of data into memory after one page fault or one miss. *See* FF 5. But this loading happens *when reading data randomly*, while claim 1 requires loading data into memory from *sequential locations* after one miss occurs. Loafman also states that if the file is being read sequentially, the process continues as customary. *Id.* Since the customary practice discussed in the Background of the Invention section (FF 3) is to wait for two misses before loading data, we find that Loafman only teaches loading with data after two misses from sequential locations.

Nor do we find that Loafman teaches that loading after one miss is well known or common knowledge in the art. *See* Ans. 14; Reply Br. 2. Loafman provides a general discussion of loading data from sequential

locations. *See* FF 3-4. While Loafman notes that loading works well for sequentially read data (FF 3), and that pre-fetching reduces the number of page faults (*id.*), Loafman nonetheless fails to suggest loading data from sequential locations after one miss (*see* FF 3-4). Notably, Loafman only provides two faults (i.e., misses) as an example of loading data from sequential locations into memory (*see id.*); Loafman provides no other examples. Loafman therefore does not suggest a finite number of identified, predictable solutions for loading the memory with data from sequential location, including loading after one miss occurs, that an ordinarily skilled artisan would have good reason to pursue. *See KSR*, 550 U.S. at 421.

The Examiner also has not sufficiently shown that an ordinarily skilled artisan would have recognized that the one-miss technique used for reading data randomly is equally applicable to reading data sequentially. The Examiner cites to Loafman's prefetching data discussion indicating pre-fetching or loading works well for sequentially reading data. *See* Ans. 8. Loafman, however, distinguishes the random reading pre-fetching technique (e.g., after one fault) from the customary sequential reading pre-fetching technique (e.g., after two faults). *See* FF 5. Thus, even accounting for the inferences and creative steps that an ordinarily skilled artisan would employ, we find that the Examiner has not established an adequate basis for concluding that Loafman would have taught or suggested loading data from sequential locations into memory after one miss occurs as recited in claim 1. *See KSR*, 550 U.S. at 418.

We therefore will not sustain the obviousness rejection of independent claim 1, and independent claim 10 which recites commensurate limitations. We likewise reverse dependent claim 2 for similar reasons.

Independent claims 5 and 13 recite similar limitations, namely “when a miss occurs, wherein after an initial miss, said line cache prevents any additional misses as long as the first CPU addresses sequential memory locations of said first memory device.” We therefore similarly find that the Examiner erred in rejecting independent claims 5 and 13, and claims 6, 7, 14, and 15 which depend from independent claims 5 and 13.

Independent claim 18 recites similar limitations to claim 1, namely that, after a first time that the requested data is not present in said cache, n pages of said cache are loaded with data from the first or second memory device’s sequential locations to prevent any additional cache misses for as long as the first and second memory device’s sequential memory locations are addressed. We therefore will not sustain the Examiner’s rejection of independent claim 18, and dependent claims 19 and 25 for similar reasons.

For the foregoing reasons, Appellants have shown error in the obviousness rejection of independent claims 1, 2, 5-7, 10, 13-15, 18, 19, and 25 based on the combination of Zaidi, Jeddalah, and Loafman.

THE REMAINING OBVIOUSNESS REJECTIONS

Claims 4, 9, 12, 17, and 20-24 are also rejected under § 103 and depend directly or indirectly from independent claims 1, 5, 10, 13, and 18. The issues are therefore the same as those discussed above in connection with independent claims 1, 5, 10, 13, and 18.

Similarly, independent claim 26 has the same limitation discussed above as claim 18. Claims 27-33 are also rejected under § 103 and depend directly or indirectly from independent claim 26. The issues are therefore the same as those discussed above with claim 18.

We therefore will not sustain the rejections of claims 4, 9, 12, 17, 20-24, and 26-33 for the foregoing reasons.

CONCLUSION

The Examiner erred in rejecting claims 1, 2, 4-7, 9, 10, 12-15, and 17-33 under § 103.

ORDER

The Examiner's decision rejecting claims 1, 2, 4-7, 9, 10, 12-15, and 17-33 is reversed.

REVERSED

DANG, *Administrative Patent Judge*, dissenting.

I respectfully dissent from my colleagues' reversal of the prior-art rejections of claims 1, 2, 4-7, 9, 10, 12-15, and 17-33 under § 103.

Appellants contend that “Zaidi, either singly or in combination of Jeddeloh and Loafman, fail to at show, teach, or suggest... said miss occurs and before a second miss occurs” (App. Br. 9) because, in Loafman, “at least two misses are required” (App. Br. 11) and “[t]he Examiner fails to provide any reference that teaches or suggests any knowledge of sequential data reading that is not based on at least two cache misses (App. Br. 13). In the Appeal Brief, Appellants define “a second” cache miss as “any additional” cache miss after an initial cache miss (App. 10-11) but state that “there will never be a miss after the initial miss” (App. Br. 10).

Appellants' argument that Loafman differs from the claimed invention because “at least two misses are required” in Loafman is not commensurate in scope with the language of the claims. That is, the language of the claims does not preclude two misses but instead requires two misses, i.e., “a miss” and “a second miss” (claim 1).

By contending that Loafman differs from the claimed invention because “at least two misses are required,” Appellants appear to be arguing that Appellants claimed invention is limited to one and only one miss since “there will never be a miss after the initial miss,” as set forth in an exemplary embodiment in the Specification. However, the language of Appellants' claims simply does not recite any such “one and only one” miss, but rather “a miss” and “a second miss.” That is, the claims do not place any limitation on what the term “a miss” is to be, is to represent, or is to

mean, other than that “said miss occurs... before a second miss occurs” (claim 1). In fact, claim 1 does not even recite a “first” or “initial” miss.

I agree with the majority’s finding that the Specification also does not define “a miss” or “a second miss” (FF 1, emphasis added). However, I will not confine “a miss” to the one and only one miss, as Appellants apparently contend as shown in an exemplary embodiment in Appellants’ Specification, when the claims do not recite a specific embodiment. Contrary to the majority, I will not read limitations into the claims from the exemplary embodiment of the Specification. *In re Van Geuns*, 988 F.2d 1181, 1184 (Fed. Cir. 1993).

Instead, absent a definition of the terms in the claims and the Specification, “the words of a claim ‘are generally given their ordinary and customary meaning.’” *Phillips v. AWH Corp.*, 415 F.3d at 1312 (Fed. Cir. 2005) (en banc) (internal citations omitted). Thus, I give the claims their broadest reasonable interpretation, consistent with the Specification, as it would be interpreted by one of ordinary skill in the art. *In re Bigio*, 381 F.3d 1320, 1324 (Fed. Cir. 2004) and *Suitco*, 2010 WL 1462294, at *4.

Accordingly, I give “a miss” its broadest reasonable interpretation as any miss that occurs before a second miss, as consistent with the definition provided in the claims. I find the language of claim 1 does not distinguish “a miss” from a miss that may occur after another miss but before a second (i.e., an additional) miss. That is, the language of claim 1 does not distinguish “a miss” from any single miss belonging to a group of two misses. Also, as consistent with the exemplary embodiment in the Specification, I interpret such claimed “miss” as any miss that will never have another miss thereafter, regardless of whether there are other misses

therebefore. That is, nothing in the claims precludes other misses occurring before the claimed miss. The language of the claims merely requires “a miss” occurring before a second miss, but is silent as to any misses before the claimed miss. Thus, I disagree with the majority and find that such interpretation of “a miss” as any miss occurring without any other misses thereafter would be consistent with the Specification and therefore reasonable. *See Suitco*, 2010 WL 1462294, at *4.

As admitted by Appellants, in *Loafman*, “at least two misses are required” (App. Br. 11). In particular, *Loafman* discloses a miss for page 202 and a miss for page 204, wherein the miss for page 204 occurs before any additional miss (FF 4). That is, there is no other miss after the miss for page 204 (FF 4-5).

I find *Loafman*’s miss for page 204 to read on Appellants’ claimed “a miss” (claim 1). That is, the miss occurs before an additional miss, as specifically defined in the claim, and there is no other miss occurring thereafter, as consistent with the exemplary embodiment set forth in the Specification. Thus, I find that Appellants’ claims do not recite any limitation to distinguish the claimed invention from such interpretation.

For the above reasons, I conclude that the Examiner did not err in finding that *Loafman* discloses the claimed “a miss” and would affirm the rejection of claim 1 and claims 2, 4-7, 9, 10, 12-15, and 17-33 falling therewith under § 103.

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